AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Cancelled)

2. (New) A method of programming a PMOS stacked-gate memory cell, wherein the memory cell includes a p-type source region in n-type semiconductor substrate, a p-type drain region formed in the n-type semiconductor substrate material and space-apart from the p-type source region to define a substrate channel region therebetween, a conductive floating gate electrode formed over the substrate channel region and separated therefrom by gate dielectric material, and a conductive control gate electrode formed over the floating gate electrode and separated therefrom by integrate dielectric material, the programming method comprising:

applying a negative voltage potential to the p-type drain region;

applying a voltage potential to the control gate electrode such that electrons are attached to the floating gate electrode from the p-type drain region through the gate dielectric material;

establishing a correlation between floating gate injection current and semiconductor substrate material current;

monitoring the value of the semiconductor substrate material current; and

utilizing the monitored value of the semiconductor substrate material current to provide a feedback correction signal to the voltage potential applied to the control gate electrode such that the semiconductor substrate material current is maximized during programming of the memory cell.

3. (New) A programming method as in claim 2, and wherein the stacked-gate memory cell is included in a memory cell array comprising a plurality of such stacked-gate memory cells

formed in n-type semiconductor substrate material, and wherein the monitored value is obtained from the memory cell array.

4. (New) A programming method as in claim 2, and wherein the stacked-gate memory cell is included in a memory cell array comprising a plurality of such stacked-gate memory cells formed in n-type semiconductor substrate material, and wherein the monitored value is obtained from a single stacked-gate memory cell.

5. (New) The programming method of claim 2, and wherein the semiconductor material is n-type silicon.

6. (New) The programming method of claim 5, and wherein the gate dielectric material is silicon dioxide.

7. (New) The programming method of claim 6, and wherein the floating gate electrode is polysilicon.

8. (New) The programming method of claim 7, and wherein the control gate electrode is polysilicon.